ELINVO (Electronics, Informatics, and Vocational Education), Mei 2021; vol 6 (1): 26-39
ISSN 2580-6424 (printed), ISSN 2477-2399 (online,) DOI: 10.21831/elinvo.v6i1.40287

A New Two-Switched-Impedance Network for High Ratio Quasi-Z-Source Inverter

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ABSTRACT

The increasing demand and widespread of renewable energy inherently compel the development of power electronics converter as an interface between consumers and the energy sources. Since the voltage generated on the typical renewable energy source such photovoltaic is low, the power converter is tasked to transform it to higher voltage level to meet load or grid voltage demand. This paper presents a new two-switched-impedance networks qZSI converter called High Ratio Two Switched-impedance quasi-Z-Source Inverter (HR2SZ-qZSI). The modification on the second cell switched-inductance structure allows this topology to achieve higher boost factor with a lower shoot-through duty ratio applied, compared with the existing two-switched-impedance-based converter family. This paper also discusses comparative analysis between the previous and the proposed topology: almost all the devices' ratings including capacitor and diode voltage, and inductor current ripple are lower than the preceding relevant two-switched-impedance qZSI family. A small-scale laboratory prototype with 20 V dc input, 0.1 shoot-through duty cycle, and 0.2 inverter index modulation was designed and tested. The experimental results which comprise 3.9 boost factor, 0.78 voltage gain, the voltage across capacitors C_1, C_2, C_3, C_4, C_5 are 32 V, 36 V, 26 V, 33 V, 32 V, respectively; the voltage stress of the diodes D_{in}, D_1, D_2, D_3, D_4, D_5 are 72 V, 8 V, 38 V, 68 V, 36 V, 36 V, respectively; and the current ripple of inductors L_1, L_2, L_3, L_4 are 0.15 A, 0.08 A, 0.13 A, 0.13 A, respectively, corroborate the theoretical analysis and the HR2SZ-qZSI operation.

Keywords: quasi-Z-Source Inverter (qZSI), voltage gain, boost factor, inductor current ripple, voltage stress

INTRODUCTION

In recent year, the potential for developing renewable energy is gaining full attention because of its abundant and non-polluting energy availability [1]–[9], especially wind and photovoltaic (PV) energy in which their installed capacity have reached 733 GW and 707 GW by end of 2020, respectively [10], [11]. PV, in particular, is attracting massive demand in commercial and residential applications globally. Unfortunately, the dc voltage generated by this energy source is very low and is highly dependent on the level of solar irradiation. In the case of AC mains connection, additional devices are needed which generally consist of a dc-dc converter and inverter [12]–[17]. The dc-dc boost converter is traditionally used to first convert the input low dc voltage to sufficient high dc voltage needed for the inverter to subsequently transform it to ac voltage required by AC grid. The major drawbacks of this configuration are it requires separate regulation of the boost converter and inverter which adds and complicates the control circuitry, the conventional Voltage Source Inverter (VSI) only works in buck mode (step down operation) and necessitates delay time for each of the leg in switching operation to prevent short circuit. In another grid-connected arrangement [16], PV generators are directly connected with both VSI and line transformer. As mentioned before, the traditional VSI limits the attainable output voltage therefore it requires the size and the turn of the transformer to adjust with the grid specification. This condition worsens the overall

performance of the power conversion system since the larger requirement of the 50/60 Hz line transformer, the bigger the dimension and cost it required.

Impedance Source Inverter or so-called Z-Source Inverter (ZSI) has emerged in the past years as a viable solution to overcome the practical difficulties mentioned earlier in renewable energy generation systems [18]. This converter consists of an X-shaped *LC*-impedance network and traditional VSI. It exhibits many superiorities over the old-fashioned use of boost dc-dc converter and line transformer since ZSI can operate in a single power conversion stage, it also enables the short circuit or shoot-through operation on each inverter's leg which additionally provide the boosting capability of the low dc voltage. Moreover, single-stage power conversion of ZSI can nullify the additional control needed in the previous classic dc-dc and dc-ac converter configuration.

Nevertheless, there are some downsides of the ZSI utilization which encompass the substantial amount of voltage stress across the capacitor, the discontinues input current owing to the series connection of input dc voltage with the power diode, and since the modulation index of the inverter is restricted to the value of the shoot-through duty cycle, the overall dc-ac voltage gain is also limited. As an effort to improve the performance operability of ZSI, quasi-Z-Source Inverter (qZSI) has been derived [19]. This topology modification includes categorical features which allow the dc side current to smoothly flow on account of series configuration between the dc voltage source and inductor, lessens the voltage held by the capacitor, provides one-point ground reference between the dc source and the converter, and limits start-up inrush current. These merits emphasize the further use of qZSI favorably in PV electricity generation [20]–[27]. Still, regarding high voltage conversion demand, qZSI offers no improvement from the former ZSI topology.

Subsequent adjustments are reported over the years to gradually improve the qZSI performance. Switched-inductor (SL) boost cells, as succeeded previously in ZSI [28], are adopted in qZSI, namely SL-qZSI and cSL-qZSI [29], [30]. Owing to the inclusion of the SL boost networks, these converters have successfully improved the boost capability of the traditional qZSI. Another interesting approach is revealed in [31]. The proposed converter Enhanced Boost qZSI or called EB-qZSI shifts the inductors and diodes position and replace one of the inductors in the two SL cells with a capacitor, hence realizes higher voltage conversion. A year after, for the dual purposes of the battery-PV application, for instance, two symmetrical structure converters are proposed, Embedded Switched-Inductor qZSI (ESL-qZSI) and improved Embedded Switched-Inductor qZSI (iESL-qZSI) [32]. Two dc sources are attached inside in each of the switched-impedance networks to maintain the continuous current flow across both sources. Yet, it is difficult to produce and control equally balanced dc input voltage in these two converters. The floating dc sources also lose the benefit of joint-ground reference in the previous qZSI, cSL-qZSI, and EB-qZSI since they need to be properly isolated before embedded in the impedance networks.

In light of the aforementioned evolution of qZSI-derived converters, this paper proposes a new High Ratio Two Switched-Impedance quasi-Z-Source Inverter (HR2SZ-qZSI). This converter put forward the new output SL boost design thus expand the output-input voltage conversion proportion. The next two sections will discuss the methodology and the results of our newly developed converter in detail.

METHODS

This section begins with revisiting the structures and electrical characteristics of the previous converter topologies: cSL-qZSI, EB-qZSI, ESL-qZSI, and iESL-qZSI. Next, the step-by-step operational procedure of the proposed HR2SZ-qZSI is thoroughly explained

and the associated mathematical analysis is expressed.

A. cSL-qZSI Topology

The continuous switched-inductor qZSI (cSL-qZSI) is shown in Fig. 1. According to [30], the output DC link, boost factor, capacitor voltage, inductor current ripple, and diode voltage are defined wherein V_{in} is a DC source, D is the value of shoot-through duty ratio, and T_S is switching period.

$$\begin{cases} V_o = \frac{1}{1-3D} V_{in} \\ B = \frac{1}{1-3D} \end{cases} \quad (1)$$

$$\begin{cases} V_{C1} = \frac{1-D}{(1+D)(1-3D)} V_{in} \\ V_{C2} = \frac{2D}{(1+D)(1-3D)} V_{in} \end{cases} \quad (2)$$

$$\begin{cases} \left|\Delta i_{L1,P-P}\right| = \frac{(1-3D^2)}{2L_1(1-2D-3D^2)} DT_S V_{in} \\ \left|\Delta i_{L2,L4,P-P}\right| = \frac{(1-D)}{2L_{2,4}(1-2D-3D^2)} DT_S V_{in} \\ \left|\Delta i_{L3,P-P}\right| = \frac{2D}{2L_3(1-2D-3D^2)} DT_S V_{in} \end{cases} \quad (3)$$

$$\begin{cases} V_{Din} = \frac{(1+D)}{(1-2D-3D^2)} V_{in} \\ V_{D1} = \frac{2D^2}{(1-3D-D^2+3D^3)} V_{in} \\ V_{D2} = V_{D5} = \frac{D}{(1-2D-3D^2)} V_{in} \\ V_{D3} = \frac{2D}{(1-2D-3D^2)} V_{in} \\ V_{D4} = \frac{(1-D)}{(1-2D-3D^2)} V_{in} \\ V_{D6} = \frac{(1-2D-D^2)}{(1-3D-D^2+3D^3)} V_{in} \end{cases} \quad (4)$$

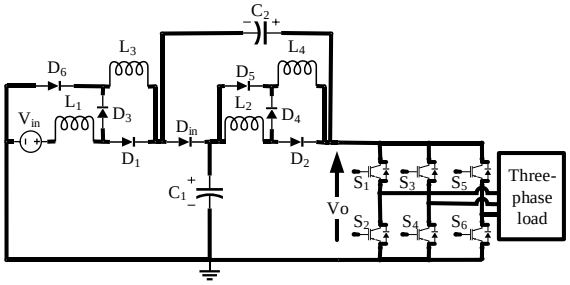

Figure 1. Topology of continuous switched-inductor qZSI (cSL-qZSI)

B. EB-qZSI Topology

Fig. 2 depicts the circuit of Enhanced Boost qZSI (Eb-qZSI). Based on the analysis in [31], the output DC link, boost factor, capacitor voltage, inductor current ripple, and diode voltage are the following:

$$\begin{cases} V_o = \frac{1}{(1-4D+2D^2)} V_{in} \\ B = \frac{1}{(1-4D+2D^2)} \end{cases} \quad (5)$$

$$\begin{cases} V_{C1} = \frac{(1-D)^2}{(1-4D+2D^2)} V_{in} \\ V_{C2} = \frac{2D-D^2}{(1-4D+2D^2)} V_{in} \\ V_{C3} = \frac{1-3D+D^2}{(1-4D+2D^2)} V_{in} \\ V_{C4} = \frac{D-D^2}{(1-4D+2D^2)} V_{in} \end{cases} \quad (6)$$

$$\begin{cases} \left|\Delta i_{L1,L2,P-P}\right| = \frac{(1-D)^2}{2L_{1,2}(1-4D+2D^2)} DT_S V_{in} \\ \left|\Delta i_{L3,L4,P-P}\right| = \frac{(1-D)}{2L_{3,4}(1-4D+2D^2)} DT_S V_{in} \end{cases} \quad (7)$$

$$\begin{cases} V_{Din} = V_{D1} = \frac{1}{(1-4D+2D^2)} V_{in} \\ V_{D2} = \frac{D}{(1-4D+2D^2)} V_{in} \\ V_{D3} = V_{D4} = \frac{(1-D)}{(1-4D+2D^2)} V_{in} \end{cases} \quad (8)$$

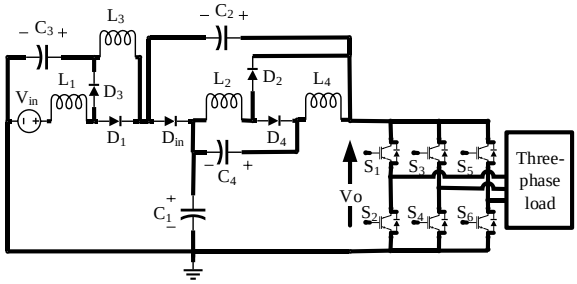

Figure 2. Topology of Enhanced Boost qZSI (EB-qZSI)

C. ESL-qZSI and iESL-qZSI Topology

Embedded switched-inductor qZSI (ESL-qZSI) and improved Embedded switched-inuctor qZSI (iESL-qZSI) schematics are portrayed in Fig. 3 and Fig. 4, respectively. The equations in (9)-(12) express the output DC link, boost factor, capacitor voltage, inductor current ripple, and diode voltage [32].

$$\begin{cases} V_o = \frac{1}{(1-4D+2D^2)} V_{in} \\ B = \frac{1}{(1-4D+2D^2)} \end{cases} \quad (9)$$

$$\begin{cases} V_{C1} = V_{C2} = \frac{1}{2(1-4D+2D^2)} V_{in} \\ V_{C3} = V_{C4} = \frac{(1-2D)}{2(1-4D+2D^2)} V_{in} \end{cases} \quad (10)$$

$$\begin{cases} \left|\Delta i_{L1,L2,P-P}\right| = \frac{(1-D)^2}{2L_{1,2}(1-4D+2D^2)} DT_S V_{in} \\ \left|\Delta i_{L3,L4,P-P}\right| = \frac{(1-D)}{2L_{3,4}(1-4D+2D^2)} DT_S V_{in} \end{cases} \quad (11)$$

$$\begin{cases} V_{Din} = \frac{1}{(1-4D+2D^2)} V_{in} \\ V_{D1} = V_{D2} = \frac{D}{(1-4D+2D^2)} V_{in} \\ V_{D3} = V_{D4} = \frac{(1-D)}{(1-4D+2D^2)} V_{in} \end{cases} \quad (12)$$

Similarly, the electrical properties of iESL-qZSI can be written as

$$\begin{cases} V_o = \frac{(1-D)}{(1-4D+2D^2)} V_{in} \\ B = \frac{(1-D)}{(1-4D+2D^2)} \end{cases} \quad (13)$$

$$\begin{cases} V_{C1} = V_{C2} = \frac{(1-D)}{2(2-8D+4D^2)} V_{in} \\ V_{C3} = V_{C4} = \frac{D}{2(2-8D+4D^2)} V_{in} \end{cases} \quad (14)$$

$$\begin{cases} \left|\Delta i_{L1,L2,P-P}\right| = \frac{(1-D)}{2L_{1,2}(1-4D+2D^2)} DT_S V_{in} \\ \left|\Delta i_{L3,L4,P-P}\right| = \frac{(1-D)^2}{2L_{3,4}(1-4D+2D^2)} DT_S V_{in} \end{cases} \quad (15)$$

$$\begin{cases} V_{Din} = \frac{(1-D)}{(1-4D+2D^2)} V_{in} \\ V_{D1} = V_{D2} = \frac{1-2D}{2(1-4D+2D^2)} V_{in} \\ V_{D3} = V_{D4} = \frac{1}{(1-4D+2D^2)} V_{in} \end{cases} \quad (16)$$

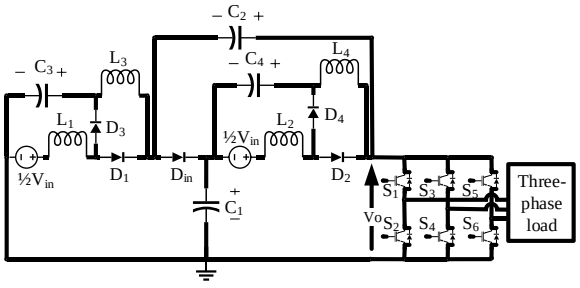

Figure 3. Topology of Embedded SL-qZSI (ESL-qZSI)

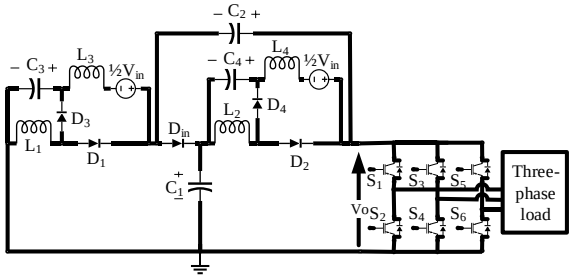

Figure 4. Topology of Embedded SL-qZSI (ESL-qZSI)

D. High Ratio Two-Switched-Impedance quasi-Z-Source Inverter (HR2SZ-qZSI)

The proposed HR2SZ-qZSI converter which consists of four inductors (L_1, L_2, L_3, and L_4), five capacitors (C_1, C_2, C_3, C_4, and C_5), and six diodes (D_{in}, D_1, D_2, D_3, D_4, and D_5), is shown in Fig. 5. The main distinction between the proposed HR2SZ-qZSI with the previous topology is the new second switched-impedance cell on the output side of HR2SZ-qZSI topology. This network consists of two capacitors (C_4 and C_5), two inductors (L_2 and L_4), and two diodes (D_2 and D_5), as shown in Fig. 5. This new output boost cell is expected to permit a more substantial boosting capacity than the older relatives of two-switched impedance networks qZSI.

E. Circuit Analysis of the Proposed HR2SZ-qZSI

The following analysis takes into account the steady-state converter characteristic, the ideal properties of the components, and both capacitance and inductance on capacitors and inductors are assumed identical. Generally, the proposed HR2SZ-qZSI has two operation modes: shoot-through (ST) state wherein one of the inverter bridges is short-circuited and the non-shoot-through (nST) wherein either one of two inverter half-bridge switches are open.

In ST state, the diodes D_1, D_2, and D_5 conduct while the rest of D_{in}, D_3, and D_4 are reverse biased, as illustrated in Fig. 6. Here, the inductor and output voltages correspond to this state can be derived as follow

$$\begin{cases} V_{L1(ST)} = V_{in}+V_{C2} \\ V_{L2(ST)} = V_{C1} = V_{C5} \\ V_{L3(ST)} = V_{C2} + V_{C3} \\ V_{L4(ST)} = V_{C5} + V_{C4} \\ V_o = 0 \end{cases} \quad (17)$$

Conversely, the diodes D_{in}, D_3, and D_4 enter conduction mode and the rest of D_1, D_2, and D_5 are turned off in NST state, as portrayed in Fig. 7. Then, expressions of the voltage across inductors and dc-link are obtained as

$$\begin{cases} V_{L1(NST)} = V_{in} - V_{C3} \\ V_{L2(NST)} = V_{C5} - V_{C4} \\ V_{L3(NST)} = V_{C3} - V_{C1} \\ V_{L4(NST)} = V_{C4} - V_{C2} \\ V_O = V_{C1} - V_{L2} + V_{C5} - V_{L4} \end{cases} \quad (18)$$

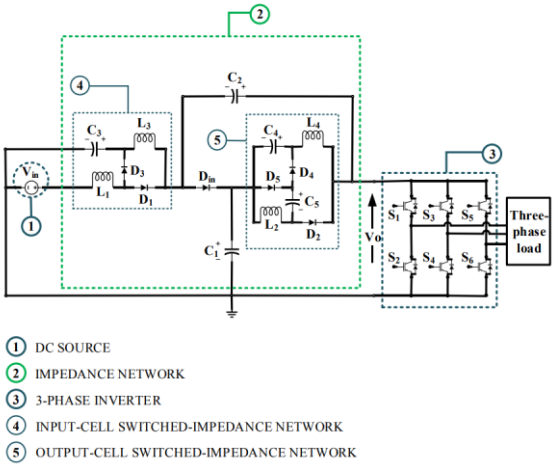

Figure 5. The Proposed Topology (HR2SZ-qZSI)

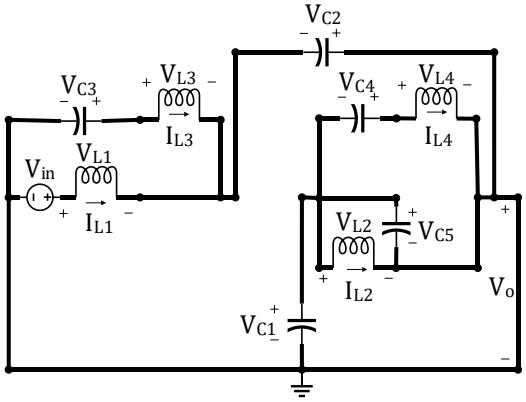

Figure 6. Shoot-through State of HR2SZ-qZSI Topology

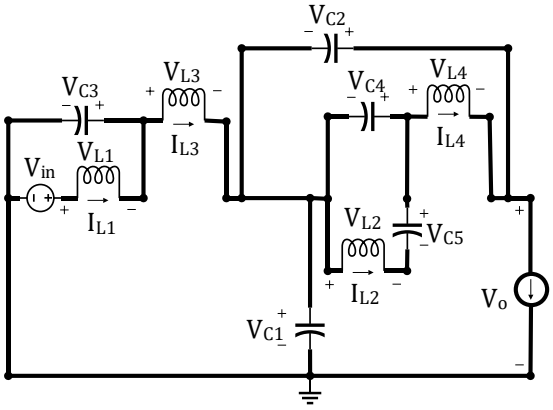

Figure 7. Non-shoot-through State of HR2SZ-qZSI Topology

After acquiring the inductor voltage expressions both in ST and NST modes, the voltage across all capacitors and the dc-link voltage can be found, as in (19), with aid of the voltage-second balance principle across all inductors in one switching period. The conversion ratio of output dc-link voltage to the input voltage, namely boost factor (B), is also derived. The voltage held by the diodes is then obtained when they are in reverse blocking mode, as expressed in (20).

$$\begin{cases} V_{C1} = V_{C5} = \frac{(1-D)^2}{(1-6D+5D^2-D^3)} V_{in} \\ V_{C2} = \frac{(1+D-D^2)}{(1-6D+5D^2-D^3)} V_{in} \\ V_{C3} = \frac{(1-4D+2D^2)}{(1-6D+5D^2-D^3)} V_{in} \\ V_{C4} = \frac{(1-D)}{(1-6D+5D^2-D^3)} V_{in} \\ V_o = \frac{(2-D)}{(1-6D+5D^2-D^3)} V_{in} = BV_{in} \\ B = \frac{(2-D)}{(1-6D+5D^2-D^3)} \end{cases} \quad (19)$$

$$\begin{cases} V_{D1} = \frac{D(2-D)}{(1-6D+5D^2-D^3)} V_{in} \\ V_{D2} = \frac{1}{(1-6D+5D^2-D^3)} V_{in} \\ V_{D5} = \frac{1-D}{(1-6D+5D^2-D^3)} V_{in} \end{cases} \quad (20)$$

$$\begin{cases} V_{Din} = \frac{2-D}{(1-6D+5D^2-D^3)} V_{in} \\ V_{D3} = \frac{(1-D)(2-D)}{(1-6D+5D^2-D^3)} V_{in} \\ V_{D4} = \frac{1-D}{(1-6D+5D^2-D^3)} V_{in} \end{cases} \quad (21)$$

RESULT AND DISCUSSION

A. Analysis of Boost Factor and Voltage Gain

Based on the boost factor on (1), (5), (9), (13), and (19), we have the comparison graph between the proposed HR2SZ-qZSI topology and the previous topology, as shown in Fig. 8. From Fig. 8, we can know that the boost factor of the proposed HR2SZ-qZSI is higher than the previous topology, and to produce that higher boost factor, the proposed HR2SZ-qZSI topology uses a lower shoot-through duty ratio.

The simple boost control (SBC) method on [18] is used to control the shoot-through state and non-shoot-through state of the proposed HR2SZ-qZSI topology. We use this method because the control structure is quite simple wherein the shoot-through state is created by the comparison of the two constant voltage that equal to or greater than the peak value of the sinewave reference. The restriction of the ST duty ratio to the modulation index follows

$$D = 1 - M \tag{22}$$

By substituting the shoot-through duty ratio (D) on (22) to the boost factor (B) of the proposed HR2SZ-qZSI on (21), we can define the boost factor as,

$$B = \frac{(2-(1-M))}{(1-6(1-M)+5(1-M)^2-(1-M)^3)} \tag{23}$$

On the output inverter side, the peak voltage of one inverter phase can be written as,

$$\hat{V}_{ph} = M\frac{V_o}{2} = MB\frac{V_{in}}{2} \tag{24}$$

From (24) and (23), we have the relation of voltage gain as follow

$$G = \frac{2\hat{V}_{ph}}{V_{in}} = MB = \frac{M^2+M}{M^3+2M^2-M-1} \tag{25}$$

By modifying the voltage gain of the previous topology, as shown in (25), then we get the comparison graph of the voltage gain between the proposed HR2SZ-qZSI and the previous topology, as shown in Fig. 9. According to this figure, we can conclude that the voltage gain of the proposed HR2SZ-qZSI topology is higher than the previous topology. In other words, to achieve the same voltage gain value as the previous topology, the proposed HR2SZ-qZSI exert a higher modulation index value hence the phase inverter voltage waveform quality can be markedly increased.

B. Capacitor and Diode Voltage Stress Analysis

To properly compare the capacitor and diode voltage stresses, the ST duty cycle of the previous converters are matched with the proposed HR2SZ-qZSI on the same voltage gain. The corresponding adjustments are listed in Table 1. Combining each capacitor and diode voltage equations for all topology, the plots of their comparison are provided in Fig. 10 and 11, respectively.

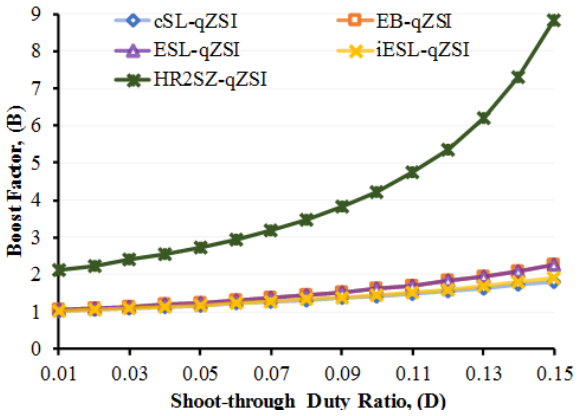

Figure 8. Boost Factor Comparison between the Proposed HR2SZ-qZSI Topology and the Previous Topology

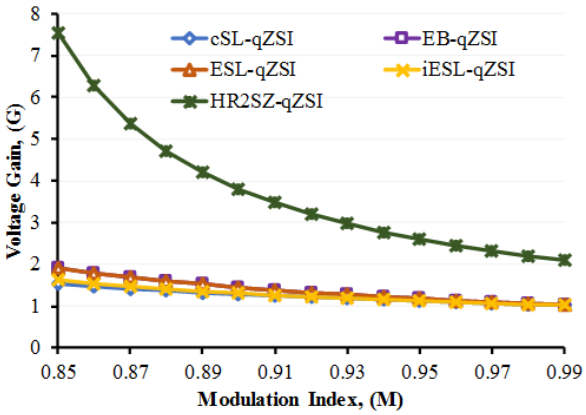

Figure 9. Voltage Gain Comparison Between the Proposed HR2SZ-qZSI Topology and The Previous Topology

From Fig. 10, we know that with the same shoot-through duty ratio, voltage stress on the C_1 of the proposed HR2SZ-qZSI is the lowest among all converters. Similarly, the voltage on C_3 on the proposed topology is the lowest, except with that of iESL-qZSI. Meanwhile, the voltage stress on C_2 and C_4 of the proposed HR2SZ-qZSI topology is relatively similar to the previous converters, but higher when compared with C_4 voltage on iESL-qZSI.

From Fig. 11, the smallest peak voltage experienced by the power diode D_{in} and D_1 when in reverse bias are found in the HR2SZ-qZSI. For D_3, D_4, and D_5, all converters have relatively equal voltage stress. However, the proposed HR2SZ-qZSI suffers the highest voltage stress on D_2.

Table 1. The Proposed HR2SZ-qZSI Shoot-through Duty Ratio Form

Topology	Shoot-through Duty Ratio, (D)
$D_{cSL\text{-}qZSI}$	$\frac{D^3-4D^2+3D+1}{D^3-2D^2-3D+5}$
$D_{EB\text{-}qZSI}$	$\frac{D^3-D^2-6D+7-\sqrt{D^6-10D^5+45D^4-110D^3+150D^2-108D+33}}{4D^2-12D+8}$
$D_{ESL\text{-}qZSI}$	$\frac{D^3-D^2-6D+7-\sqrt{D^6-10D^5+45D^4-110D^3+150D^2-108D+33}}{4D^2-12D+8}$
$D_{iESL\text{-}qZSI}$	$\frac{D^3-D^2-6D+7-\sqrt{D^6-10D^5+45D^4-110D^3+150D^2-108D+33}}{4D^2-12D+8}$
$D_{HR2SZ\text{-}qZSI}$	$\frac{(1-D)(2-D)}{(1-6D+5D^2-D^3)}$

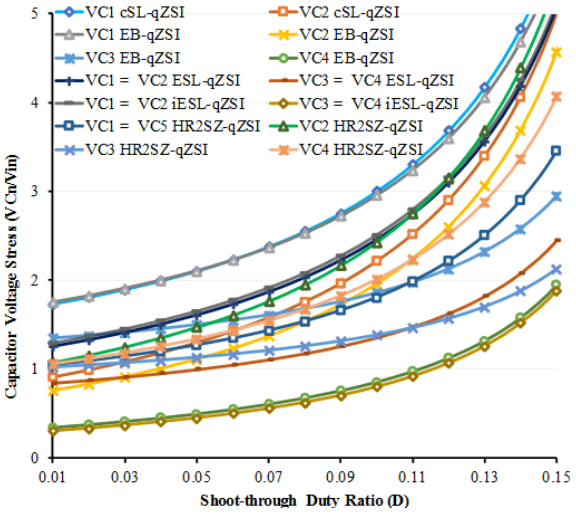

Figure 10. Capacitor voltage stress comparison between the proposed HR2SZ-qZSI topology and the previous topology

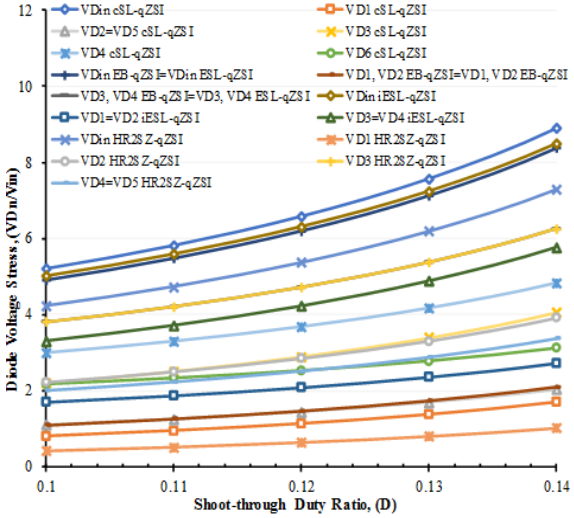

Figure 11. Diode voltage stress comparison between the proposed HR2SZ-qZSI topology and the previous topology

C. Analysis of Inductor Current Ripple

The inductor voltage V_{Ln} expression is given in (26), where n indicates the suitable inductor position based on the circuit in Fig. 5.

$$V_{Ln} = L_n \frac{di_{Ln}}{dt} \tag{26}$$

The peak-to-peak inductor current or current ripple is expressed by substituting (26) and (19) to (17) or (18). Note that the inductor current rose and fell every half of the switching frequency thus the absolute value of the inductor current ripple for both ST and NST states are identical. The following equations represent the corresponding absolute ripple on the inductor currents,

$$\begin{cases} \left|\Delta i_{L1,P-P}\right| = \frac{(2-D)(1-D)^2}{2L_1(1-6D+5D^2-D^3)} DT_S V_{in} \\ \left|\Delta i_{L2,P-P}\right| = \frac{(1-D)^2}{2L_2(1-6D+5D^2-D^3)} DT_S V_{in} \\ \left|\Delta i_{L3,P-P}\right| = \frac{(1-D)(2-D)}{2L_3(1-6D+5D^2-D^3)} DT_S V_{in} \\ \left|\Delta i_{L4,P-P}\right| = \frac{(1-D)(2-D)}{2L_4(1-6D+5D^2-D^3)} DT_S V_{in} \end{cases} \tag{27}$$

From those, we get the comparison graph of the inductor current ripple between the proposed HR2SZ-qZSI topology with the previous topology by substituting $D_{topology}$ from Table I into the inductor current ripple on (3), (7), (11), (15), and (27), as shown in Fig. 12. As demonstrated in this figure, the proposed

HR2SZ-qZSI has the best characteristic since the current ripples on all the inductors were the lowest between all relevant two-switched-impedance-based qZSI.

D. Simulation Results

To clearly understand the operation of the proposed topology and to test all the previous associated formulae, circuit simulation based on Fig. 5 is conducted in PSIM with the parameter detail is provided in Table 2. The converter is performed using SBC modulation technique as previously mentioned in the analysis.

Fig. 13 shows the line voltage, phase voltage, and phase current waveforms. The value of filtered peak phase voltage is 380 V and its rms voltage is 219 V and the load current is around 4.38 A. The steady state capacitor voltage waveforms are depicted in the next figure. We obtain V_{C1} = V_{C5} = 165 V, V_{C2} = 255 V, V_{C3} = 101 V, and V_{C4} = 192 V from Fig. 14. From Fig. 15, the output voltage and diode voltage are V_o = 421 V, V_{Din} = 420 V, V_{D4} = V_{D5} = 193 V, V_{D1} = 64 V, V_{D2} = 226 V, and V_{D3} = 357 V. Both inductor current waveforms and their ripple are presented in Fig. 16. This figure delineates the current ripple profile such are $|\Delta i_{L1,\,P\text{-}P}|$ = 6.81 A, $|\Delta_{iL2,\,P\text{-}P}|$ = 3.68 A, and $|\Delta i_{L3,\,P\text{-}P}|$ = $|\Delta i_{L4,\,P\text{-}P}|$ = 8.02 A.

The simulation has offered clarity and verification of the proposed HR2SZ-qZSI topology. For instance, according to (19), the calculated dc-link voltage is 424.62 V and gives an 8.846 boost factor. According to the simulation, they are 421 V and 8.77, respectively. Similar conformities for capacitor and diode voltage, the phase inverter voltage, and the current ripple are also found with the prior mathematical analysis in (20), (21), (24), and (27).

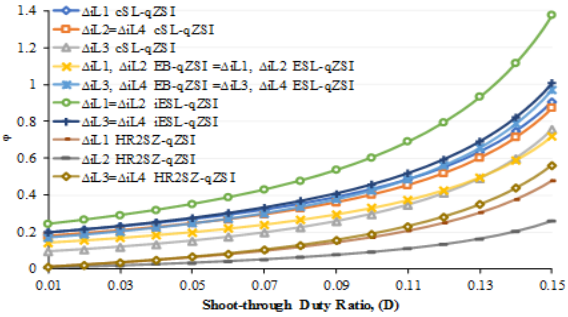

Figure 12. Current ripple inductor comparison between the proposed HR2SZ-qZSI topology and the previous topology

Table 2. Simulation Parameter

No.	Parameter	Rating
1.	DC source, (V_{in})	48 V_{DC}
2.	Inductor, (L_1=L_2=L_3=L_4)	330 µH
3.	Capacitor, (C_1=C_2=C_3=C_4=C_5)	470 µF
4.	Switching frequency, (f_s)	10 kHz
5.	Inverter frequency (f)	50 Hz
6.	Modulation index, (M)	0.85
7.	Shoot-through duty ratio, (D)	0.15
8.	Output filter, (L_f and C_f)	1.5 mH, 10 µF
9.	Load	50 Ω

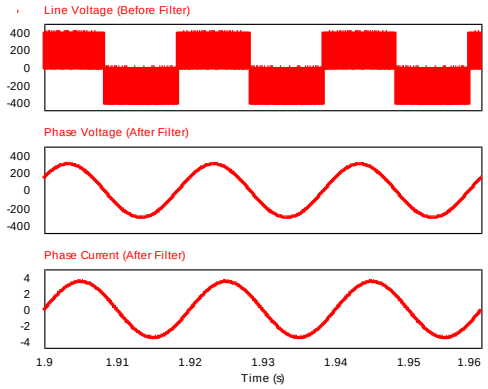

Figure 13. Voltage waveforms before and after *LC* Output Filter and Phase Current After Filter

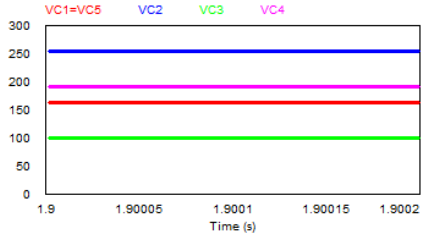

Figure 14. Capacitor voltage simulation waveforms for V_{C1}, V_{C2}, V_{C3}, V_{C4}, and V_{C5}

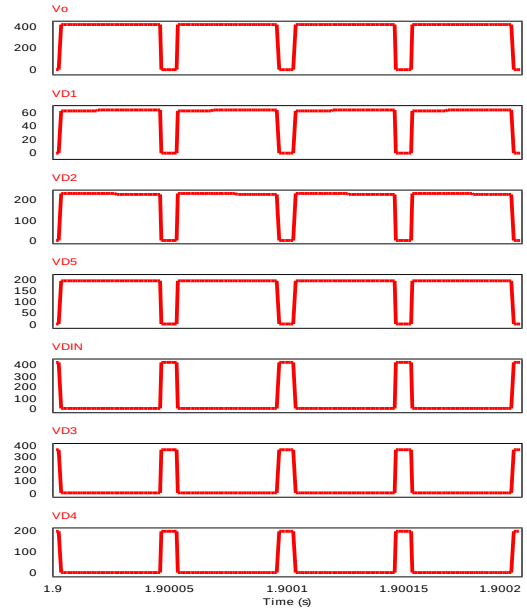

Figure 15. Simulation waveform of dc-link output voltage V_o and voltage across diodes V_{Din}, V_{D1}, V_{D2}, V_{D3}, V_{D4}, and V_{D5}

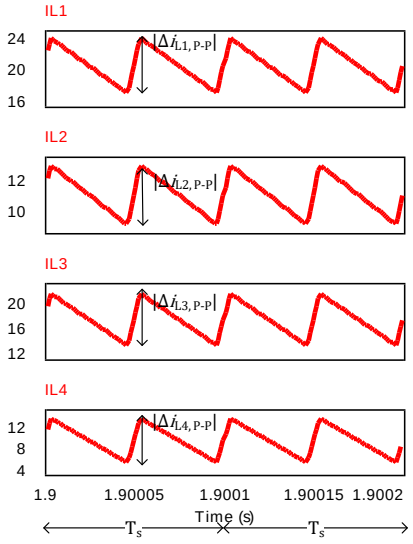

Figure 16. Simulation result of the inductor currents and their respective ripples

E. Experimental Results

A small-scale laboratory prototype is built to examine the practical ability of the proposed HR2SZ-qZSI. In the experiment, the SBC modulation method is constructed using TMS320F28335 microcontroller. Following the configuration in Fig. 5, the rest of the experiment detail is given in Table 3. The low modulation index is regulated at 0.2 to restrict the power output of the inverter since the low value resistor of 50 Ω is utilized. Similarly, the input voltage is scaled down to 20 Vdc instead of 48 Vdc used in the previous simulation.

The experimental waveforms of output dc-link voltage, the inverter line voltage before and after output LC filter, are shown in Fig. 17-20. According to (19) and parameters in Table 3, the calculated dc-link output voltage, V_o, is 84.63 V. We can notice there is a slight difference from the experiment waveform from Fig. 17 where V_o is around 78 V. Similarly, the inverter phase voltage and peak line-to-line voltage can be derived from (24) and calculated by multiplying (24) by √2, yielding 8.46 Vrms and 14.66 Vrms, respectively. The experimental results from these two parameters can be observed from Fig. 19 and 20. The peak of phase and line-to-line inverter voltage from experiment are 7 Vrms and 12 Vrms, respectively.

Table 3. Parameter of the Laboratory Experiment

No.	Parameter	Rating
1.	DC source, (V_{in})	20 V_{DC}
2.	Inductor, (L_1=L_2=L_3=L_4)	2.5 mH
3.	Capacitor, (C_1=C_2=C_3=C_4=C_5)	470 µF
4.	Switching frequency, (f_s)	10 kHz
5.	Inverter frequency (f)	50 Hz
6.	Modulation index, (M)	0.2
7.	Shoot-through duty ratio, (D)	0.1
8.	Output filter, (L_f and C_f)	1.5 mH, 10 µF
9.	Load	50 Ω

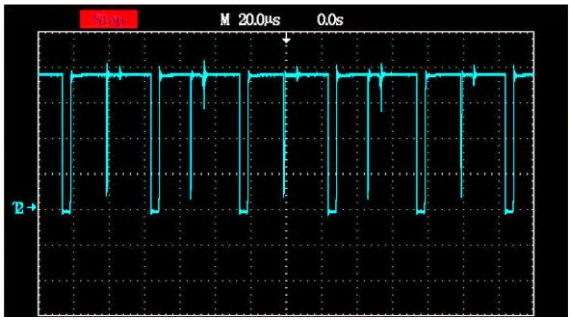

Figure 17. Experimental waveform of the output dc link V_o (20 V/div, 20µs/div)

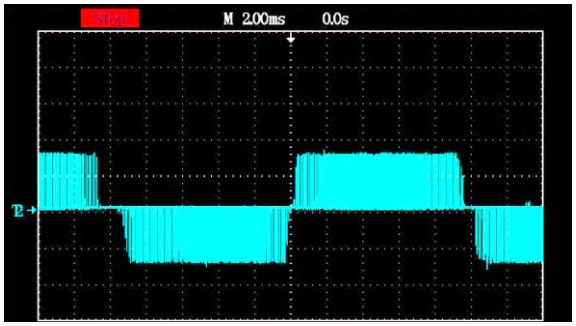

Figure 18. Experimental waveform of the inverter line voltage V_{ab} (50 V/div, 2ms/div)

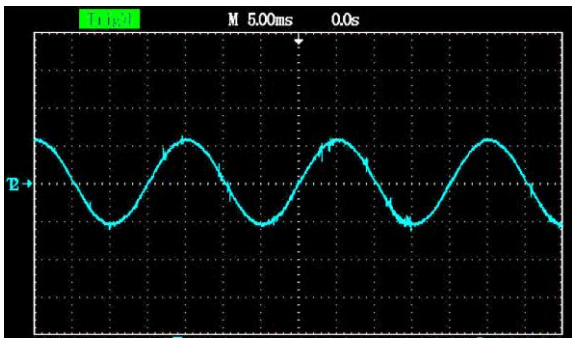

Figure 19. Experimental waveform of the inverter line voltage V_{ab} after output LC filter (10 V/div, 5ms/div)

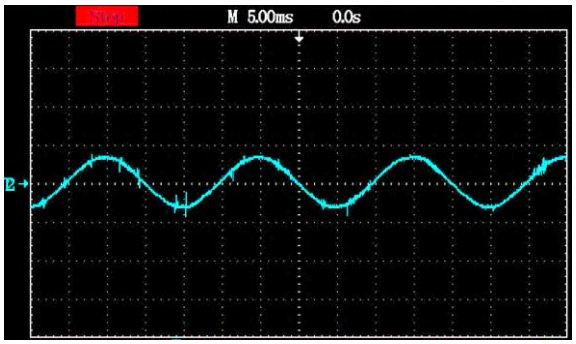

Figure 20. Experimental waveform of the inverter phase voltage V_{ph} after output LC filter (10 V/div, 5ms/div)

In the case of voltage across capacitors and diodes, they can be derived from (19)-(21). From these formulae, the value of V_{C1}, V_{C2}, V_{C3}, V_{C4}, and V_{C5}, are 36.08 V, 48.55 V, 27.62 V, 40.08 V, and 36.08 V, respectively. These results correspond with the experiment waveforms, as depicted in Fig. 21-24, wherein the voltage held by C_1, C_2, C_3, C_4, and C_5, are approximately 32 V, 36 V, 26 V, 33 V, and 32 V, respectively. Fig. 25-30 shows the waveforms of voltage stress across diode D_{in}, D_1, D_2, D_3, D_4, and D_5, in which their respective values are 76 V, 8 V, 38 V, 68 V, 36 V, and 34 V, respectively. The laboratory experiments of peak stress voltage across the diodes when in reverse biased condition, justify the associated mathematical analysis in (20) and (21), wherein V_{Din}, V_{D1}, V_{D2}, V_{D3}, V_{D4}, and V_{D5} are 84.63 V, 8.46 V, 44.54 V, 76.17 V, 40.09 V, and 40.09 V, respectively.

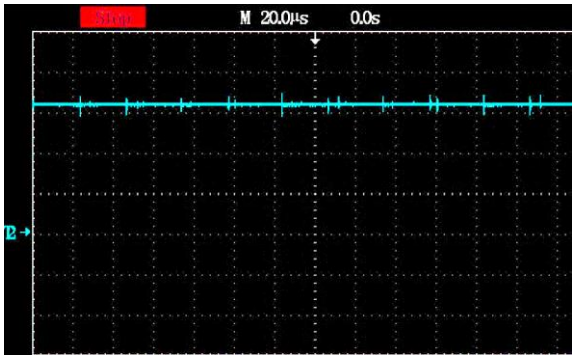

Figure 21. Experimental waveform of the capacitor voltage $V_{C1} = V_{C5}$ (10 V/div, 20µs/div)

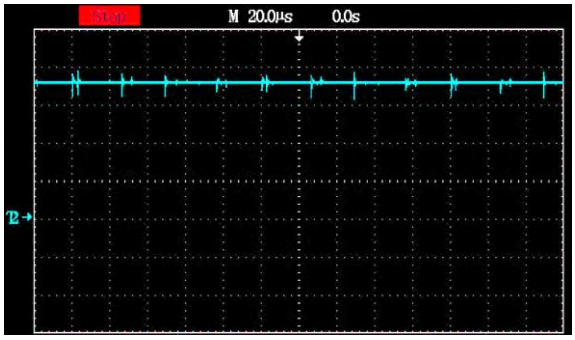

Figure 22. Experimental waveform of Capacitor Voltage V_{C2} (10 V/div, 20µs/div)

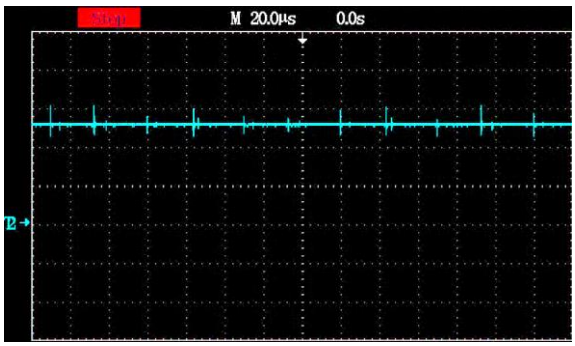

Figure 23. Experimental waveform of Capacitor Voltage V_{C3} (10 V/div, 20µs/div)

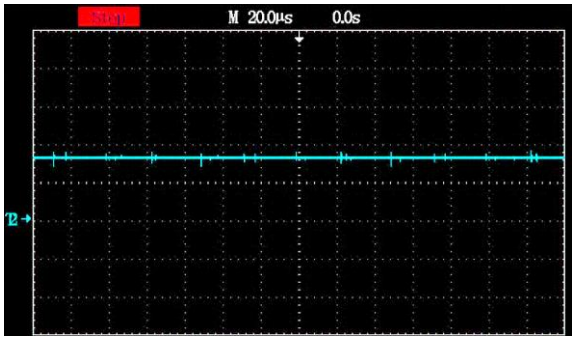

Figure 24. Experimental waveform of Capacitor Voltage V_{C4} (20 V/div, 20µs/div)

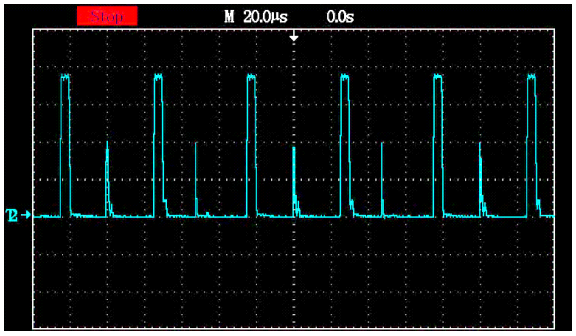

Figure 25. Experimental waveform of diode voltage V_{Din} (20 V/div, 20µs/div)

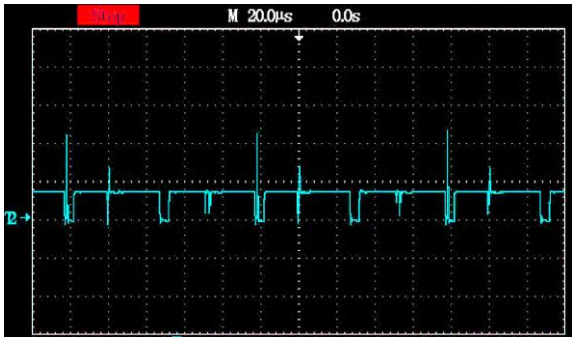

Figure 26. Experimental waveform of diode voltage V_{D1} (10 V/div, 20µs/div)

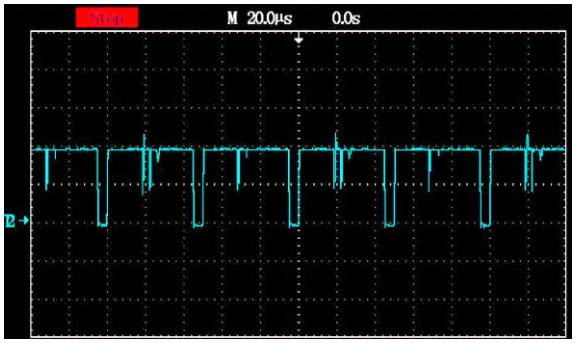

Figure 27. Experimental waveform of diode voltage V_{D2} (20 V/div, 20µs/div)

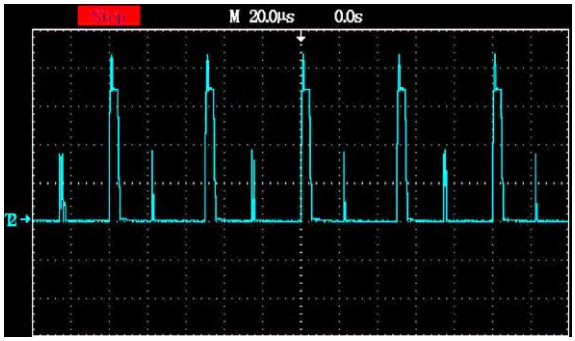

Figure 28. Experimental waveform of diode voltage V_{D3} (20 V/div, 20µs/div)

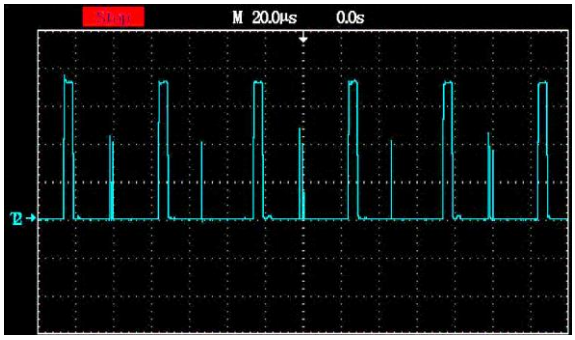

Figure 29. Experimental waveform of diode voltage V_{D4} (10 V/div, 20µs/div)

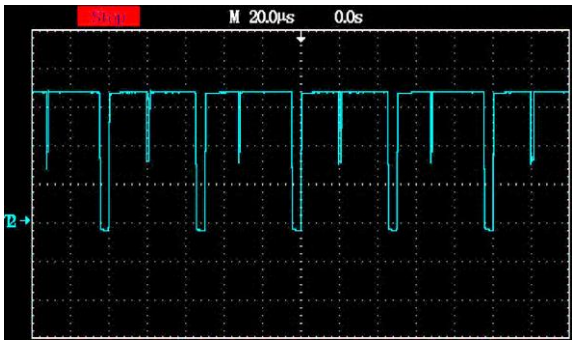

Figure 30. Experimental waveform of diode voltage V_{D5} (10 V/div, 20µs/div)

Fig. 31-34 shows the inductor current experiment waveforms and their related ripple profiles. The current ripple for each inductor L_1, L_2, L_3, and L_4, are roughly 0.15 A, 0.08 A, 0.13 A, and 0.13 A, and they closely match with the calculation from (27), in which $\Delta i_{L1,\,P\text{-}P} = 0.13$ A, $\Delta_{iL2,\,P\text{-}P} = 0.7$ A, and $\Delta i_{L3,\,P\text{-}P} = \Delta i_{L4,\,P\text{-}P} = 0.15$ A. Table 4 reports the comparison between all important parameters between mathematical analysis: (19)-(21), (24) and (27), and with the experiment findings. We can conclude both data are quite agreeable despite the lower value on experimental voltage due to the lossy parasitic components. Aside from the occasional voltage or current spike due to the components' non-

ideality, all experiment findings have closely matched with the simulation waveforms characteristic demonstrated in Fig. 13-16. Therefore, the experiment of the proposed HR2SZ-qZSI has corroborated both the previous pertinent theoretical analysis and its converter operability.

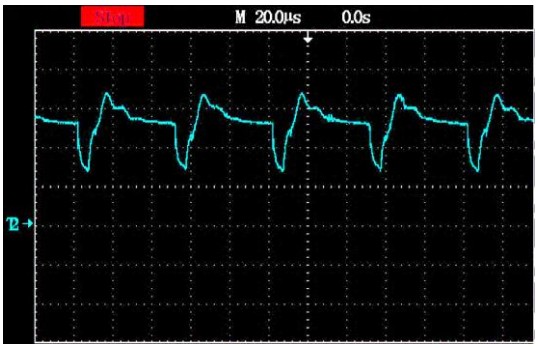

Figure 31. Experimental waveform of inductor current i_{L1} (2 V/div, 46.5 mA/V, 20µs/div)

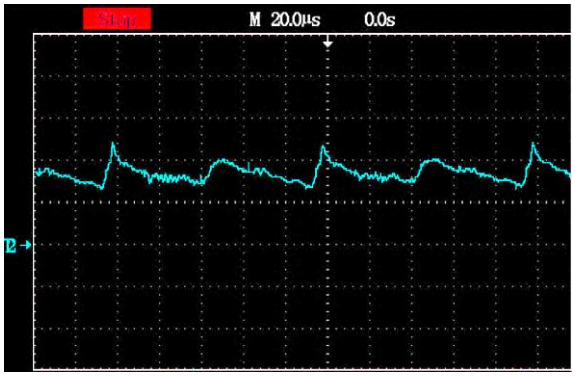

Figure 32. Experimental waveform of inductor current i_{L2} (1 V/div, 93 mA/V, 20µs/div)

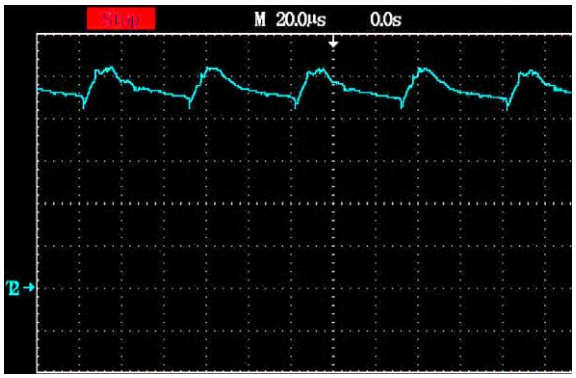

Figure 33. Experimental waveform of inductor current i_{L3} (2 V/div, 46.5 mA/V, 20µs/div)

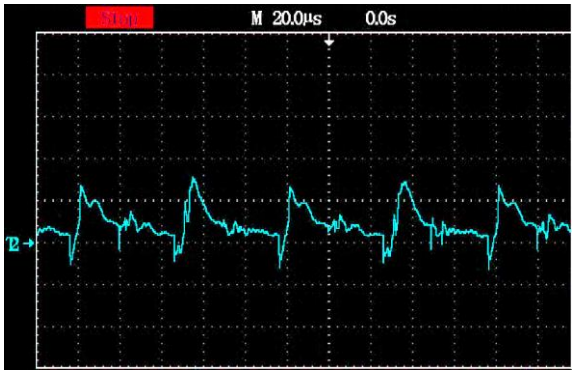

Figure 34. Experimental waveform of inductor current i_{L4} (1 V/div, 93 mA/V, 20µs/div)

Table 4. Numerical comparison between theoretical analysis and laboratory experiment

No.	Key Parameter	Theoretical	Experiment
1.	V_o	84.63 Vpeak	78 Vpeak
2.	B	4.23	3.9
3.	G	0.846	0.78
4.	V_{ph}	8.46 Vrms	7.0 Vrms
5.	V_{ab}	14.66 Vrms	8.48 Vrms
6.	V_{C1}	36.08 V	32 V
7.	V_{C2}	48.55 V	36 V
8.	V_{C3}	27.62 V	26 V
9.	V_{C4}	40.09 V	33 V
10.	V_{C5}	36.08 V	32 V
11.	V_{Din}	84.63 V	76 V
12.	V_{D1}	8.46 V	8 V
13.	V_{D2}	44.54 V	38 V
14.	V_{D3}	76.17 V	68 V
15.	V_{D4}	40.09 V	36 V
16.	V_{D5}	40.09 V	34 V
17.	$\Delta i_{L1,\,P\text{-}P}$	0.13 A	0.15 A
18.	$\Delta i_{L2,\,P\text{-}P}$	0.07 A	0.08 A
19.	$\Delta i_{L3,\,P\text{-}P}$	0.15 A	0.13 A
20.	$\Delta i_{L4,\,P\text{-}P}$	0.15 A	0.13 A

CONCLUSION

This paper has explained the proposal of the HR2SZ-qZSI topology. It features a higher boost factor and voltage gain with a lower shoot-through duty cycle and high value of modulation index. From the comparative analysis point of view, the proposed HR2SZ-qZSI evidence lower stress on capacitors, diodes, and inductor current ripples compared to the two-switched-impedance converter family, cSL-qZSI, EB-qZSI, ESL-qZSI, and iESL-qZSI. The corresponding theory about the proposed topology has been substantiated with the

computer simulation and downscale laboratory experiment. The experiments with dc input voltage of 20 V, 0.1 ST duty cycle, and 0.2 modulation index have proved the proposed converter operation along with the respective important calculated parameters. Interestingly, this proposed converter preserves the inherent features of the conventional qZSI: common ground point between the dc source and converter and smooth input current operation, hence it clearly a suitable inverter choice for renewable energy venture.

ACKNOWLEDGEMENT

We greatly appreciate the State University of Malang for funding this research work through the PNBP Research Grant Scheme.

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